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George Claseman

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Dorsey & Whitney LLP

US Bank Center

1420 Fifth Avenue

Suite 3400

Seattle, WA 98101-4010

EXAMINER

SAVLA, ARPAN P

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/849,749	<b>Applicant(s)</b> CLASEMAN, GEORGE	
	<b>Examiner</b> Arpan P. Savla	<b>Art Unit</b> 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-6,8-13,16,18,20-22 and 25-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-6,8-13,16,18,20-22 and 25-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### Response to Amendment

This Office action is in response to Applicant's communication filed March 14, 2008 in response to the Office action dated November 14, 2007. Claims 2, 3, 5, 6, 8, 10, 12, 13, 16, 18, 20-22, and 25 have been amended. Claims 1, 14, 15, and 17 have been canceled. Claims 2-6, 8-13, 16, 18, 20-22, and 25-29 are pending in this application.

## OBJECTIONS

### Drawings

1. In view of Applicant's amendment, the objection to the drawings is withdrawn.

## REJECTIONS BASED ON PRIOR ART

### Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 2-6, 8-13, 16, 18, 20, 22, and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Don Pannell, "Clause 22 Access to Clause 45 Registers" (hereinafter "Pannell") in view of Law et al., "IEEE P802.3ae 10Gb/s**

**Ethernet MDC/MDIO Proposal” (hereinafter “Law”) and Nick Parlante, “Pointers and Memory” (hereinafter “Parlante”).**

4. **As per claim 5**, Pannell discloses a method for expanding addressing capability of a plurality of registers and connected to an interface comprising:

designating at least two of the plurality of registers as a block of registers (pg. 14, the “65,536 Registers”); *It should be noted that the 65,536 registers comprise at least one “block of registers”*

providing a plurality of such blocks of registers (pg. 14, the “65,536 Registers”);  
designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers (pg. 14, the “Addr Reg”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the “Addr Reg” is analogous to the “first register.” It should also be noted that the Addr Reg is used to address (i.e. characterize) the block of 65,536 Registers.*

and designating a second register within the plurality of registers that is separate from the blocks of registers for specifying at least one operation for the indicated block of registers (pg. 14, the “C45 R/W Control”; pg. 10, the “Management Frame Fields - Clause 45” table). *It should be noted that the “C45 R/W Control” is analogous to the “second register.” It should also be noted that the “opcode” stored in C45 R/W Control specifies at least one operation for the block of 65,536 Registers.*

Pannell does not disclose wherein said first register comprises a pointer to a plurality of location registers, each of the plurality of location registers indicating at least one such block of registers;

wherein said second register comprises a pointer to a plurality of control registers, each of the plurality of control registers comprising an operational code;

and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operational code is associated with a second of such blocks of registers.

Law discloses each of the plurality of location registers indicating at least one such block of registers (Slide 5, registers 2 and 3);

each of the plurality of control registers comprising an operational code (Slide 5, registers 0 and 9; Slide 9, "OP");

and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operational code is associated with a second of such blocks of registers (Slide 9, "OP"). *It should be noted that the control registers are associated with the location registers and that all control registers contain "opcode" (i.e. "OP").*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose wherein said first register comprises a pointer to a plurality of location registers,

wherein said second register comprises a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1<sup>st</sup> paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2<sup>nd</sup> paragraph).

Therefore, it would have been obvious to combine Pannell, Law, and Parlante for the benefit of obtaining the invention as specified in claim 5.

5. **As per claim 2**, the combination of Pannell/Law/Parlante discloses the first register includes a block selector for selectively characterizing at least one of such blocks of registers as an indicated block of registers (Pannell, pg. 14, the “Device Select” signal). *It should be noted that the Device Select signal sent to the C45 R/W Control and then eventually to the Addr Reg effectively acts as a “block selector” for the Addr Reg.*

6. **As per claim 3**, the combination of Pannell/Law/Parlante discloses the second register includes an operational code (Pannell, pg. 14, the “the Opcode” being sent to the C45 R/W Control). *It should be noted that “Opcode” is analogous to “operational code.”*

7. **As per claim 4**, the combination of Pannell/Law/Parlante discloses the second register includes a port indicator (Pannell, pg. 14, the “Port Select” signal). *It should be noted that the Port Select signal sent to the MUX, then AND gate, and eventually to the C45 R/W Control effectively acts as a “port indicator” for the C45 R/W Control.*

8. **As per claim 6**, the combination of Pannell/Law/Parlante discloses said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22 (Pannell, pg. 25).

9. **As per claim 20**, Pannell discloses a system for expanding the addressing capability of a plurality of registers, the system comprising:

a plurality of blocks of registers, each block of registers having at least two registers (pg. 14, the “65,536 Registers”);

a location register separate from the plurality of blocks of registers for selectively characterizing at least one of the blocks of registers as a specified block of registers (pg. 14, the “Addr Reg”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the “Addr Reg” is analogous to the “location register.”*

a control register separate from the plurality of blocks of registers for selecting at least one operational code for the specified block of registers and specifying at least one port number for the specified block of registers (pg. 14, the “C45 R/W Control”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the “C45 R/W Control” is analogous to the “control register.”*

and a control engine operable to access the operational code for the specified block of registers and act on the specified block of registers at each of the specified port numbers in accordance with the operational code (pg. 14, the “Existing Clause 22 STA”). *It should be noted that the “Existing Clause 22 STA” is analogous to the “control engine.” It should be noted that the STA (station management) accesses and controls the PHY (physical layer interface). Thus, it is inherently required the STA access and control the block of 65,536 Registers within the PHY in accordance with the Opcode signal.*

Pannell does not disclose wherein said location register includes a pointer to a plurality of location registers, each indicating a register block;



and wherein said control register includes a pointer to a plurality of control registers, each of the plurality of control registers storing a respective operational code, and wherein said plurality of locations registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a block.

Law discloses said location register indicates a register block (Slide 5, registers 2 and 3);

and each of the plurality of control registers storing a respective operational code (Slide 5, registers 0 and 9; Slide 9, "OP"), and wherein said plurality of locations registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a block (Slide 9, "OP"). *See the citation note for the similar limitation in claim 5 above.*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose wherein said location register includes a pointer to a plurality of location registers;

and wherein said control register includes a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1<sup>st</sup> paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2<sup>nd</sup> paragraph).

Therefore, it would have been obvious to combine Pannell, Law, and Parlante for the benefit of obtaining the invention as specified in claim 20.

10. **As per claim 8**, the combination of Pannell/Law/Parlante discloses each of the respective operational codes specifies an operation to be performed on the specified block of registers (Law, Slide 9, "OP" and "Access Type" table).

11. **As per claim 9**, the combination of Pannell/Law/Parlante discloses the operation is restricting the specified block of registers to read operations only (Law, Slide 9, OP "10, Read").

12. **As per claim 10**, the combination of Pannell/Law/Parlante discloses the respective operational codes specify control sequencing information (Law, Slide 9, OP “11, Post Read Inc Address”).

13. **As per claim 11**, the combination of Pannell/Law/Parlante discloses the control sequencing information instructs the control engine to proceed to a next block after completing operations with the specified block (Law, Slide 9, OP “11, Post Read Inc Address”).

14. **As per claim 12**, the combination of Pannell/Law/Parlante discloses said location register includes a block selector indicating said block. (Pannell, pg. 14, the “Device Select” signal). *See the citation note for claim 2 above.*

15. **As per claim 13**, the combination of Pannell/Law/Parlante discloses said location register includes a pointer to a block selector (Pannell, pg. 14, the “Device Select signal”; Parlante, pg. 3, 1<sup>st</sup> paragraph).

16. **As per claim 16**, the combination of Pannell/Law/Parlante discloses said control register is further operable to store a register indicator indicative of a register within said block (Pannell, pg. 14, the signal sent from the “C45 R/W Control” to the “Addr Reg”). *It should be noted that the Addr Reg gets all its information from the C45 R/W Control, therefore, because the Addr Reg addresses the block of 65,536 Registers, it is inherently required the C45 R/W Control stores register addresses (i.e. register indicators) of registers within the block of 65,536 Registers.*

17. **As per claim 18**, the combination of Pannell/Law/Parlante discloses said control register is operable to specify a plurality of ports (Pannell, pg. 7, line 5; pg. 14, the “5 Port Address Pins” and the “Port Select” signal).

18. **As per claim 22**, the combination of Pannell/Law/Parlante discloses said location and control registers are registers specified by IEEE standard 802.3 clause 22 (Pannell, pg. 25).

19. **As per claim 26**, Pannell discloses a method for expanding addressing capability of a plurality of registers, comprising:

designating at least two of the plurality of registers as a block of registers (pg. 14, the “65,536 Registers”);

providing a plurality of such blocks of registers (pg. 14, the “65,536 Registers”);

designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers (pg. 14, the “Addr Reg”; pg. 10, the “Management Frame Fields - Clause 45” table);

designating a second register within the plurality of registers that is separate from the blocks of registers for specifying at least one operation for the indicated block of registers (pg. 14, the “C45 R/W Control”; pg. 10, the “Management Frame Fields - Clause 45” table). *See the citation notes for the same limitations in claim 5 above.*

Pannell does not disclose the first register including a pointer to a plurality of location registers that each indicates at least one of the blocks of registers;

the second register including a pointer to a plurality of control registers in which each control register includes an operational code;

and associating said plurality of location registers with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operation code is associated with a second of such blocks of registers.

Law discloses each location register indicates at least one of the blocks of registers (Slide 5, registers 2 and 3);

and each control register includes an operational code (Slide 5, registers 0 and 9; Slide 9, "OP");

and associating said plurality of location registers with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operation code is associated with a second of such blocks of registers (Slide 9, "OP"). *See the citation note for the similar limitation in claim 5 above.*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the

predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose the first register including a pointer to a plurality of location registers;

and the second register including a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1<sup>st</sup> paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2<sup>nd</sup> paragraph).

Therefore, it would have been obvious to combine Pannell, Law, and Parlante for the benefit of obtaining the invention as specified in claim 26.

20. **As per claim 27**, the combination of Pannell/Law/Parlante discloses the first register includes a block selector for selectively characterizing at least one of such blocks of registers as an indicated block of registers (Pannell, pg. 14, the "Device Select" signal). *See the citation note for claim 2 above.*

21. **As per claim 28**, the combination of Pannell/Law/Parlante discloses the second register includes a port indicator (Pannell, pg. 14, the “Port Select” signal). *See the citation note for claim 4 above.*

22. **As per claim 29**, the combination of Pannell/Law/Parlante discloses said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22 (Pannell, pg. 25).

**Claim 21 is rejected under 35 U.S.C. 103(a) as being obvious over Pannell in view of Law and Parlante as applied to claim 20 above, and further in view of Tsushima et al. (U.S. Patent 5,872,989) (hereinafter “Tsushima”).**

24. **As per claim 21**, the combination of Pannell/Law/Parlante discloses all the limitations of claim 21 except said operational code each encode an operation selected from the group of operations consisting of pointer handling and stream looping.

Tsushima discloses said operational code each encode an operation selected from the group of operations consisting of pointer handling and stream looping (col. 6, lines 9-23; col. 7, lines 22-34; Fig. 9; Fig. 11).

The combination of Pannell/Tsushima/Pannell and Tsushima are analogous art because they are from the same field of endeavor, that being memory systems using registers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Tsushmia’s read and write pointers (known technique) to Pannell/Law/Parlante's 802.3 system (a known system) ready for improvement to yield

the predictable results of handling a large capacity physical register file even if the register specifying field in the instruction is small.

Therefore, it would have been obvious to combine Pannell/Law/Parlante and Tsushima for the benefit of obtaining the invention as specified in claim 21.

**25. Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Pannell in view of Law and Parlante as applied to claim 20 above, and further in view of Webb et al. (U.S. Patent 5,694,587) (hereinafter “Webb”).**

The combination of Pannell/Law/Parlante discloses a location register (Pannell, pg. 14, the “Addr Reg”).

The combination of Pannell/Law/Parlante does not disclose a mask register following the location register and specifying a mask for the specified block of registers.

Webb discloses a mask register specifying a mask (col. 6, line 67 – col. 7, line 3; col. 7, lines 40-42).

The combination of Pannell/Law/Parlante and Webb are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Webb’s mask register within Pannell/Law/Parlante’s 802.3 system.

The motivation for doing so would have been to allow fast access to mask (Webb, col. 7, line 41).

Therefore, it would have been obvious to combine Pannell/Law/Parlante and Webb for the benefit of obtaining the invention as specified in claim 25.



**Response to Arguments**

26. The indicated allowability of **claims 5, 20, and 26-29** is withdrawn in view of the newly discovered reference to Law. Rejections based on the newly cited reference appear above. Accordingly, this action is made non-final.

**Conclusion**

**STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 2-6, 8-13, 16, 18, 20-22, and 25-29** have received a third action on the merits and are subject of a third action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2185

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/

Examiner, Art Unit 2185

July 20, 2008

/Hong Kim/

Primary Examiner, Art Unit 2185